PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10043458	01/09/2002	716		2825	

**APPLICANTS: Teng Chin-Chi; Dai Wei-Jin;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☒	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		SILI 2282
Verified and Acknowledged Examiners's intials			

TITLE : Clock tree synthesis for a hierarchically partitioned IC layout

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED: Total Claims	Print Claim for O.G
ISSUE FEE: Amount Due	Date Paid		DRAWING: Sheets Drwg.	Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAIMER		Primary Examiner	Application Examiner	
		PREPARED FOR ISSUE		

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